400G QSFP-DD LR4 Transceiver

Overview

The Wave2Wave 400G QSFP-DD LR4 Transceiver is a long-reach optical module designed for modern data center, cloud, and carrier networks that require reliable 400G performance over single-mode fiber. Using a 4-lane CWDM architecture and compliant with QSFP-DD MSA and 100G Lambda MSA, it supports transmission distances up to 10 km with strong signal integrity.



Equipped with EML lasers, PIN receivers, and an 8×53.125G PAM4 (400GAUI-8) electrical interface, the module delivers efficient 400G optical transport with low power consumption and stable thermal performance. Compliant with IEEE 802.3cu and 100G Lambda MSA 400G-LR4-10., it ensures seamless interoperability across next-generation switching and routing platforms within a 0°C to 70°C operating range.

Features & Benefits

- Compliant with QSFP-DD MSA Type 2, 100G Lambda MSA 400G LR4, and IEEE 802.3bs.
- Supports 400Gb/s transmission over 4 CWDM lanes up to 10 km on SMF.
- Utilizes EML transmitters and PIN receivers for high stability and long-reach performance.
- Integrates 8×53.125G PAM4 electrical lanes (400GAUI-8) for seamless system compatibility.
- Efficient operation with a single +3.3V supply and ≤9W power consumption.
- Designed for reliable performance across 0–70°C commercial temperature range.
- Built with a duplex LC connector and fully RoHS compliant.
- QSFP-DD MSA rev 5.0 compliant and CMIS 4.0

Applications

- 400G Ethernet
- Data center and cloud interconnects
- Leaf-spine architectures
- Long-reach switching and routing links
- High-capacity AI/ML and HPC networks

Ordering information

Part Number	Transmitter	Output Power	Receiver	Receive power	Reach	Temp	DDM	RoHS
77-QD040-LR4	CWDM EML	-2.8 to +4 dBm	PIN	-9.1 to +4 dBm	10 km	0 to 70 ºC	Available	Compliant

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Notes
Storage Temperature	Ts	-40	85	ºC	
Relative Humidity	RH	10	85	%	Non-condensing
Supply Voltage	Vcc	-0.5	3.6	V	
Damage threshold, each lane	THd	4.5		dBm	1

Recommended Operating Conditions						
Parameter	**Symbol**	**Min.**	**Typical**	**Max.**	**Unit**	**Notes**
Operating Case Temperature (Commercial)	TC	0		70	ºC	
Supply Voltage	Vcc	3.135	3.3	3.465	V	
Electrical interface data rate, each lane (PAM4)			26.5625 ± 100 ppm		GBd	
Link distance over G.652 single mode fiber	D	0.002		10	km	

Transmitter Optical Characteristics						
Parameter	**Symbol**	**Min.**	**Typical**	**Max.**	**Unit**	**Notes**
PAM4 signaling rate, each lane			53.125 ± 100 ppm		GBd	
Lane wavelengths (range)	λ0	1264.5	1271	1277.5	nm	
	λ1	1284.5	1291	1297.5	nm	
	λ2	1304.5	1311	1317.5	nm	
	λ3	1324.5	1331	1337.5	nm	
Side-mode suppression ratio	SMSR	30			dB	
Total average launch power				9.5	dBm	
Average launch power, each lane	Pa	-2.8		4	dBm	1
Outer optical modulation amplitude, each lane	OMAouter	0.2		4.2	dBm	2
Launch power in OMAouter minus TDECQ, each lane, for ER ≥ 4.5 dB		-1.2			dB	
Launch power in OMAouter minus TDECQ, each lane, for ER < 4.5 dB		-1.1			dB	
Transmitter and dispersion eye closure for PAM4, each lane	TDECQ			3.9	dB	
Difference in launch power between any two lanes (OMAouter)				4	dB	
Extinction ratio	ER	3.5			dB	
RIN17.1OMA	RIN			-136	dB/Hz	
Optical return loss tolerance	TOL			17.1	dB	
Transmitter reflectance	TRL			-26	dB	3
Average launch power of OFF transmitter, each lane	Poff			-20	dBm	

NOTES:

1. Average launch power, each lane (min) is informative and is not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; a value above this does not by itself ensure compliance.
2. The OMAouter minimum applies at low TDECQ. At higher TDECQ the launch power in OMAouter minus TDECQ rows above govern.
3. Transmitter reflectance is defined looking into the transmitter.

Receiver Optical Characteristics						
Parameter	**Symbol**	**Min.**	**Typical**	**Max.**	**Unit**	**Notes**
PAM4 signaling rate, each lane			53.125 ± 100 ppm		GBd	
Lane wavelengths (range)	λ0	1264.5	1271	1277.5	nm	
	λ1	1284.5	1291	1297.5	nm	
	λ2	1304.5	1311	1317.5	nm	
	λ3	1324.5	1331	1337.5	nm	
Damage threshold, each lane	THd	4.5			dBm	1
Average receive power, each lane		-9.1		4	dBm	2
Receive power, each lane (OMAouter)				4.2	dBm	
Difference in receive power between any two lanes (OMAouter)				4.1	dB	
Receiver reflectance				-26	dB	
Receiver sensitivity (OMAouter), each lane (max)				max(-6.6, SECQ - 8.0)	dBm	3
LOS assert	LOSA	-20			dBm	
LOS de-assert	LOSD			-8.6	dBm	
LOS hysteresis	LOSH	0.5			dB	
Conditions of stressed receiver sensitivity test						
Stressed eye closure for PAM4 (SECQ), lane under test	SECQ	0.9		3.4	dB	4
OMAouter of each aggressor lane			1.5		dBm	
Long term performance						
BER floor			1E-6 at -3.1 to 2 dBm			5

NOTES:

1. The receiver shall tolerate, without damage, continuous exposure to an optical signal at this average power level. The receiver is not required to operate correctly at this input power.
2. Average receive power, each lane (min) is informative and is not the principal indicator of signal strength. A received power below this value cannot be compliant; a value above this does not by itself ensure compliance.
3. Receiver sensitivity (OMAouter), each lane (max) is informative and is defined for a transmitter with SECQ up to 3.4 dB. Sensitivity shall meet RS = max(-6.6, SECQ - 8.0) dBm, illustrated in Figure 1.
4. Measured with a conformance test signal at TP3 for BER = 2.4E-4.
5. Long term performance is measured under recommended operating conditions.

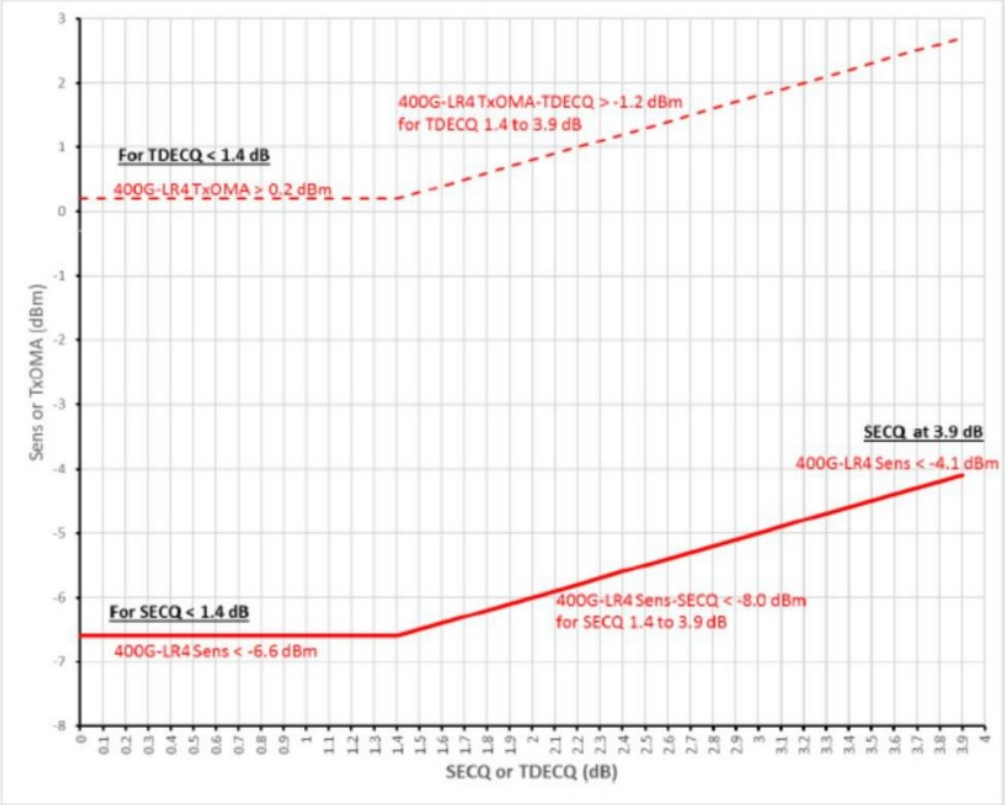


Figure 1. Illustrated of receiver sensitivity mask for 400G LR4

Digital Diagnostic Monitoring						
Performance item	**Alarm and warning flags**	**Alarm and warning thresholds**	**Monitor value**	**Performance item**	**Alarm and warning flags**	**Alarm and warning thresholds**
Module temperature	Lower page 9	Page 2h (128-135)	Lower page (14-15)	Module temperature	Lower page 9	Page 2h (128-135)
Module voltage	Lower page 9	Page 2h (136-143)	Lower page (16-17)	Module voltage	Lower page 9	Page 2h (136-143)
Bias current	Page 11h (143-146)	Page 2h (184-191)	Page 11h (170-177)	Bias current	Page 11h (143-146)	Page 2h (184-191)
Transmitter optical power	Page 11h (139-142)	Page 2h (176-183)	Page 11h (154-161)	Transmitter optical power	Page 11h (139-142)	Page 2h (176-183)
Receiver optical power	Page 11h (149-152)	Page 2h (192-199)	Page 11h (186-193)	Receiver optical power	Page 11h (149-152)	Page 2h (192-199)

Electrical Characteristics						
Parameter	**Symbol**	**Min.**	**Typical**	**Max.**	**Unit**	**Notes**
Module supply current	Icc			2860	mA	
Power dissipation	PD			9	W	
Transmitter (module electrical input, TP1)						
Signaling rate, each lane			26.5625 ± 100 ppm		GBd	
Input differential impedance	ZIN		100		Ω	
Overload differential input voltage, pk-pk		900			mV	
DC common mode voltage		-350		2850	mV	3
Single-ended voltage tolerance range		-0.4		3.3	V	
Differential termination mismatch				10	%	at 1 MHz
Differential input return loss (SDD11)		OIF-CEI-56G-VSR-PAM4 Equation (16-1)			dB	
Common mode to differential mode conversion (SCD11)		OIF-CEI-56G-VSR-PAM4 Equation (16-2)			dB	
Module stressed input test		See OIF-CEI-56G-VSR-PAM4 16.3.10.3 and IEEE 802.3bs 120E.3.4.1				1, 2
Receiver						
Signaling rate, each lane			26.5625 ± 100 ppm		GBd	
Output differential impedance			100		Ω	
Differential data output swing, pk-pk				900	mV	
AC common mode output voltage, RMS				17.5	mV	
Differential termination mismatch				10	%	at 1 MHz
Differential output return loss (SDD22)		OIF-CEI-56G-VSR-PAM4 Equation (16-1)			dB	
Common mode to differential mode conversion (SDC22)		OIF-CEI-56G-VSR-PAM4 Equation (16-3)			dB	
Common mode return loss (SCC22)				-2	dB	250 MHz to fb
Transition time		9.5			ps	
Near-end eye width at 1E-6 probability (EW6)		0.265			UI	
Near-end eye height at 1E-6 probability (EH6)		70			mV	
Far-end eye width at 1E-6 probability (EW6)		0.20			UI	
Far-end eye height at 1E-6 probability (EH6)		30			mV	
Near-end eye linearity		0.85				

NOTES:

1. With the exception to IEEE 802.3bs 120E.3.1.2 that the pattern is PRBS31Q or scrambled idle
2. Meets BER specified in IEEE 802.3bs 120E.1.1
3. DC common mode voltage generated by the host. Specification includes effects of ground offset voltage

Regulatory Compliance

Feature	Agency	Standard	Performance
Safety	NRTL	UL 62368-1, CAN/CSA C22.2 No. 62368-1, IEC 60825-1, IEC 60825-2	NRTL recognized component for US and Canada
	TUV	EN 62368-1, EN 60825-1, EN 60825-2	TUV certificate
	FDA	U.S. 21 CFR 1040.10 and 1040.11	FDA/CDRH certified with accession number, per Laser Notice 56
Electromagnetic compatibility	Radiated emissions	EMC Directive 2014/30/EU, EN 55032, CISPR 32, FCC 47 CFR Part 15, ICES-003, VCCI-CISPR 32, AS/NZS CISPR 32	Class B digital device with a minimum -6 dB margin to the limit when tested in a metal enclosure. Final margin varies with system application; good system EMI practice is required to achieve Class B at the system level. Tested 30 MHz to 40 GHz or the 5th harmonic, whichever is less.
	ESD	EMC Directive 2014/30/EU, EN 55035, CISPR 35, IEC/EN 61000-4-2	Withstands discharges of +/-8 kV contact and +/-15 kV air
	Radiated immunity	EMC Directive 2014/30/EU, EN 55035, CISPR 35, IEC/EN 61000-4-3	Field strength of 10 V/m from 80 MHz to 6 GHz
Restriction of hazardous substances	RoHS	EU RoHS (2011/65/EU and (EU) 2015/863), UK RoHS, EN IEC 63000:2018, BS EN IEC 63000:2018	Compliant

Pin Description

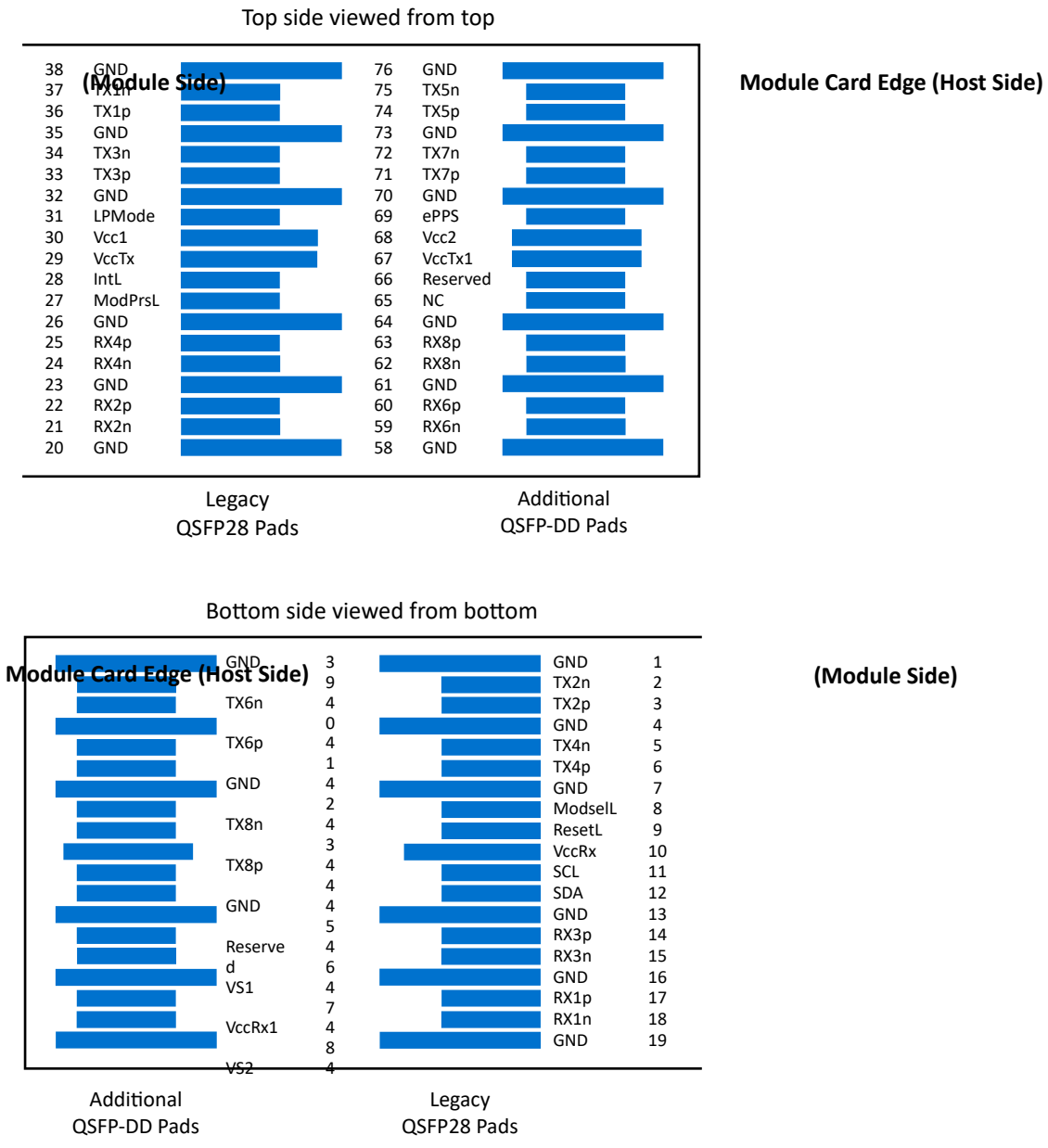
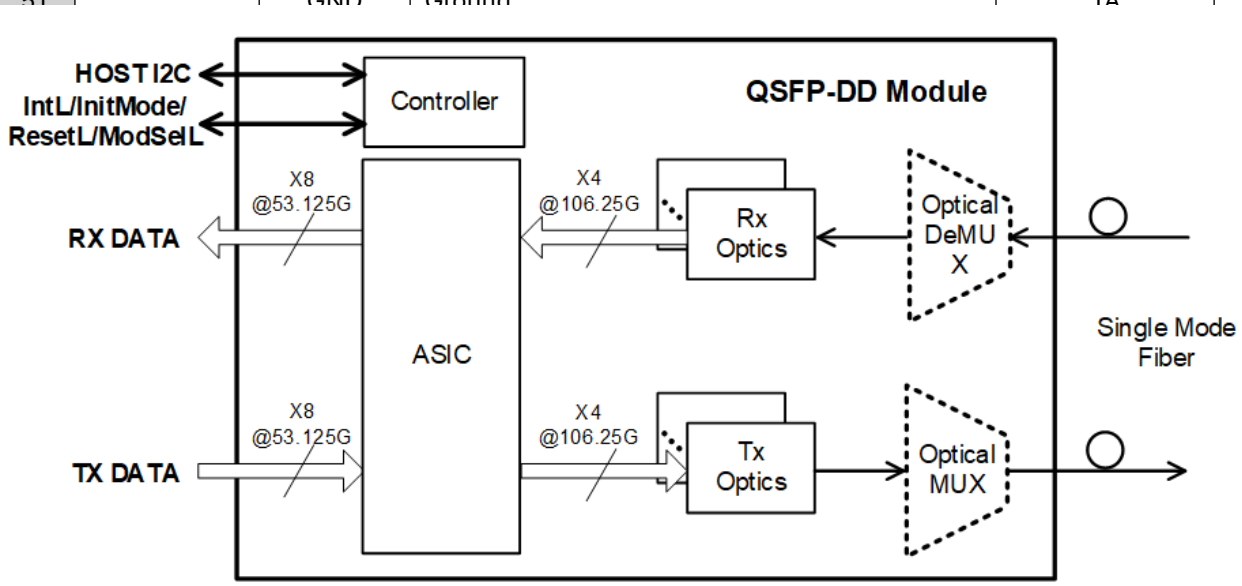


Figure 2. QSFP-DD pad assignment top view

PIN Description					
Pin	Logic	Symbol	Name/Description	Plug Sequence	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL	Interrupt	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	LPMode	Low Power mode	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1
39		GND	Ground	1A	1

PIN Description (continued)					
Pin	Logic	Symbol	Name/Description	Plug Sequence	Notes
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		VS1	Module Vendor Specific 1	3A	3
48		VccRx1	3.3V Power Supply	2A	2
49		VS2	Module Vendor Specific 2	3A	3
50		VS3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52		GND	Ground	1A	1
53	CML-O	Rx3n	Receiver Inverted Data Output	3A	
54	CML-O	Rx3p	Receiver Non-Inverted Data Output	3A	
55		GND	Ground	1A	1
56	CML-O	Rx1n	Receiver Inverted Data Output	3A	
57	CML-O	Rx1p	Receiver Non-Inverted Data Output	3A	
58		GND	Ground	1A	1
59	CML-O	Rx4n	Receiver Inverted Data Output	3A	
60	CML-O	Rx4p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx2n	Receiver Inverted Data Output	3A	
63	CML-O	Rx2p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		VccRx2	3.3V Power Supply	2A	2
66		VccHost	3.3V Power Supply	2A	2
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69	LVTTL-I	ePPS	Precision Time Protocol (PTP) reference clock input	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1



NOTES:

1. QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 8. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. For power classes 4 and above the module differential loading of input voltage pins must not result in exceeding pin current limits. The connector Vcc pins are each rated for a maximum current of 1000 mA.
3. All Vendor Specific, Reserved, No Connect and ePPS (if not used) pins may be terminated with 50 ohm to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 k⍰ and less than 100 pF.
4. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A and 1B will then occur simultaneously, followed by 2A and 2B, followed by 3A and 3B

Transceiver Block Diagram

Figure 3. Example QSFP-DD Host Board Schematic for Optical Modules

Mechanical Specifications

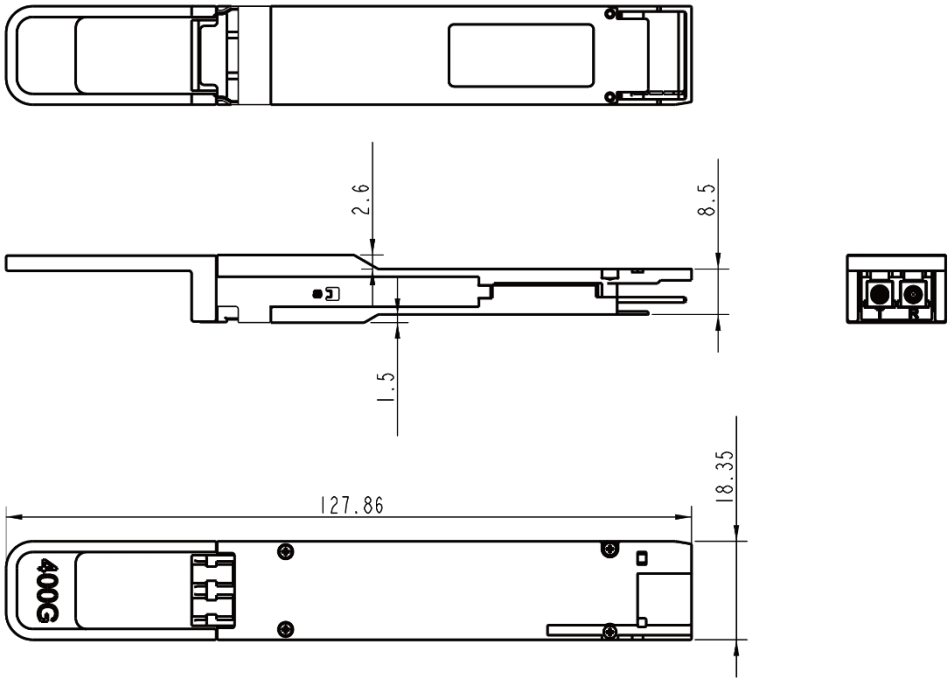


Figure 4. Outline Drawing