400G QSFP112 to 2x200G QSFP112 AEC
Active Electrical Cable

Overview

The Wave2Wave 400G QSFP112 to 2×200G QSFP112 Active Electrical Cable (AEC) is engineered for next-generation data center, cloud, and AI infrastructures that demand high bandwidth, low latency, and exceptional signal integrity. This AEC enables efficient 400G to dual-200G breakout, delivering reliable performance across high-density switching, routing, and compute environments. Fully aligned with the latest IEEE and QSFP112 MSA standards, it provides a power-efficient, plug-and-play interconnect optimized for modern 112G PAM4 architectures.



Features & Benefits

- Compliant with IEEE 802.3ck, QSFP112 MSA, and CMIS 5.2.
- Supports 400G → 2×200G breakout over 4×112G PAM4 lanes.
- Cable options 26–34 AWG with reach up to 7 m.
- Post-FEC BER < 1×10^{-15} for high signal integrity.
- Low-power 3.3V operation for dense deployments.
- Reliable within 0–70°C temperature range.
- Active design ensures low latency and high throughput.
- RoHS compliant for environmental standards.

Applications

- Hyperscale and enterprise data centers
- AI and ML compute clusters
- Cloud infrastructure platforms
- Networking equipment including switches, routers, servers, and storage
- High-performance computing environments
- Edge and core network architectures

Absolute Maximum Ratings

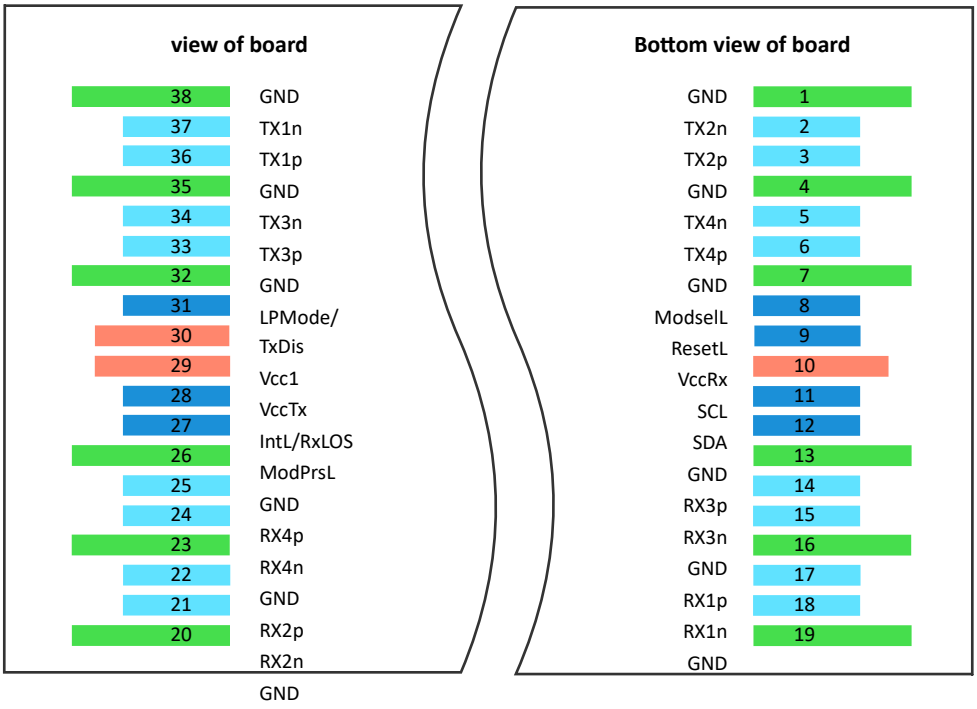
Parameter	Unit	Min.	Typical	Max.	Notes
Storage Temperature	ºC	-45		80	
Operating Relative Humidity	%			85	
Power Supply not Damaged Voltage	V	-0.5		3.6	

Recommended Operating Conditions

Parameter	Unit	Min.	Typical	Max.	Notes
Operating Case Temperature	ºC	0		70	
Power Supply Working Voltage	V	3.135	3.3	3.465	
Bit Rate	Gbps		400		

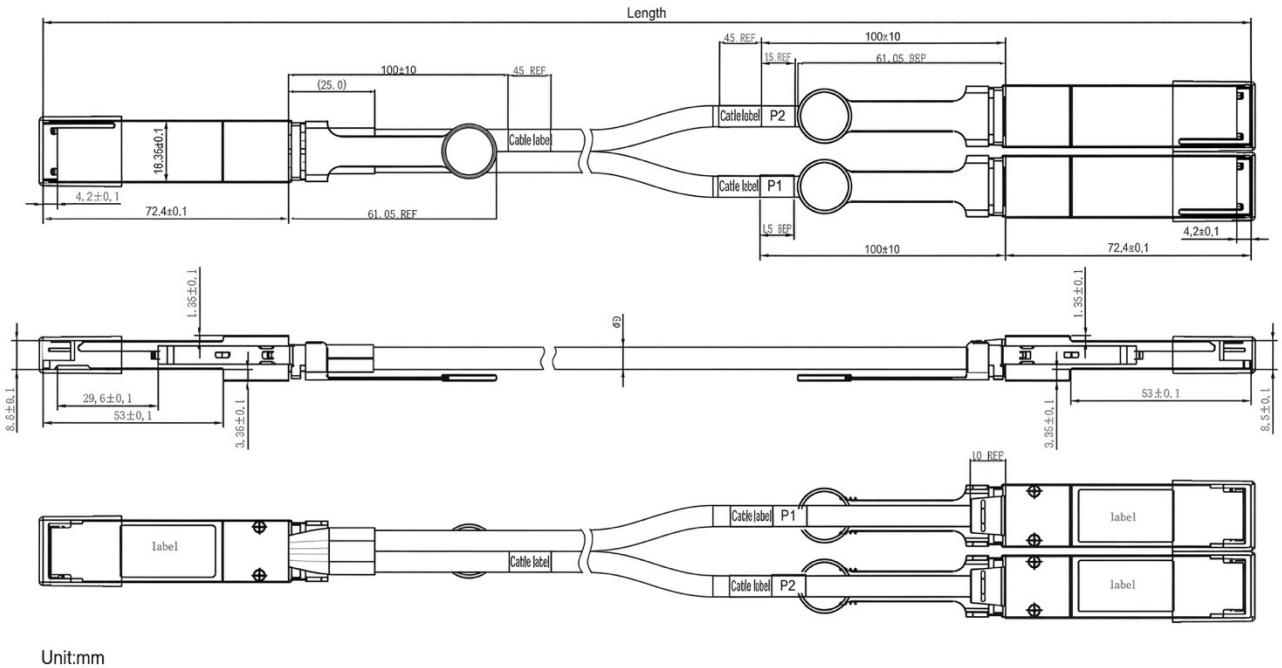
PIN Function Definitions				
Pin #	Symbol	Level/Logic	Description	Notes
1	GND		Module Ground	
2	Tx2n	CML-I	Transmitter Inverted Data Input	
3	Tx2p	CML-I	Transmitter Non-Inverted Data Input	
4	GND		Module Ground	
5	Tx4n	CML-I	Transmitter Inverted Data Input	
6	Tx4p	CML-I	Transmitter Non-Inverted Data Input	
7	GND		Module Ground	
8	ModSelL	LVTTL-I	Module Select	
9	ResetL	LVTTL-I	Module Reset	
10	VccRx		+3.3V Power Supply for Receiver	
11	SCL	LVTTL-I	2-Wire Serial Interface Clock	
12	SDA	LVTTL-I/O	2-Wire Serial Interface Data Line	
13	GND		Module Ground	
14	Rx3p	CML-O	Receiver Non-Inverted Data Output	
15	Rx3n	CML-O	Receiver Inverted Data Output	
16	GND		Module Ground	
17	Rx1p	CML-O	Receiver Non-Inverted Data Output	
18	Rx1n	CML-O	Receiver Inverted Data Output	
19	GND		Module Ground	
20	GND		Module Ground	
21	Rx2n	CML-O	Receiver Inverted Data Output	
22	Rx2p	CML-O	Receiver Non-Inverted Data Output	
23	GND		Module Ground	
24	Rx4n	CML-O	Receiver Inverted Data Output	
25	Rx4p	CML-O	Receiver Non-Inverted Data Output	
26	GND		Module Ground	
27	ModPrsL	LVTTL-O	Module Present	
28	IntL/RxLOSL	LVTTL-O	Interrupt. Optionally configurable as RxLOSL via the management interface	
29	VccTx		+3.3V Power Supply for Transmitter	
30	Vcc1		+3.3V Power Supply	
31	LPMode/TxDis	LVTTL-I	Low Power Mode. Optionally configurable as TxDis via the management interface	
32	GND		Module Ground	
33	Tx3p	CML-I	Transmitter Non-Inverted Data Input	
34	Tx3n	CML-I	Transmitter Inverted Data Input	
35	GND		Module Ground	
36	Tx1p	CML-I	Transmitter Non-Inverted Data Input	
37	Tx1n	CML-I	Transmitter Inverted Data Input	
38	GND		Module Ground	

Electrical Pad Layout



Mechanical Outlines

For detail mechanical information, please refer to the related document of QSFP-DD MSA.



Unit:mm

EEPROM Information

The digital diagnostic memory map specific data field defined as following. For detail EEPROM information, please refer to the related document of CMIS5.2.

