400G QSFP112 to 400G QSFP112 AEC
Active Electrical Cable

Overview

The Wave2Wave 400G QSFP112 to 400G QSFP112 Active Electrical Cable (AEC) delivers high-performance 400G connectivity for modern data center, cloud, and AI infrastructures. Supporting advanced 112G PAM4 architectures, it provides a stable, low-latency link between switches, servers, and storage systems requiring consistent 400Gb/s throughput.

Fully compliant with IEEE 802.3ck and QSFP112 MSA, this AEC ensures seamless interoperability across next-generation networks. Its active electrical design extends reach, improves signal integrity, and maintains power efficiency through a single 3.3V supply. With plug-and-play integration and reliable thermal performance, it supports dense fabrics, high-capacity switching, and performance-driven environments.



Features & Benefits

- Compliant with IEEE 802.3ck, QSFP112 MSA, and CMIS 5.2.
- Supports full 400Gb/s operation over 4×112G PAM4 electrical lanes.
- Cable gauge options 26–34 AWG with link lengths up to 7 meters.
- Post-FEC BER < 1×10^{-15}, ensuring high-integrity transmission.
- Efficient 3.3V single-supply power design for dense environments.
- Stable operation across 0–70°C case temperature range.
- Active electrical architecture provides low latency and extended reach.
- RoHS compliant, meeting global environmental requirements.

Applications

- Hyperscale and enterprise data centers
- AI and machine-learning compute clusters
- Cloud infrastructure and virtualized environments
- High-capacity switches, routers, and servers
- Storage and HPC platforms
- Edge and core network environments

Absolute Maximum Ratings

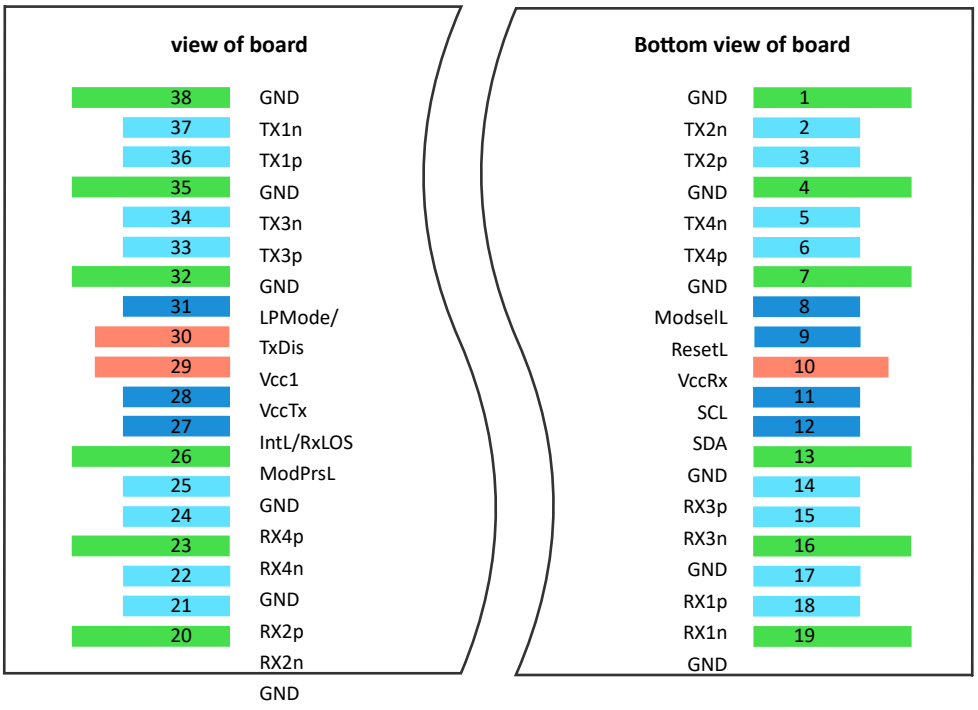
Parameter	Unit	Min.	Typical	Max.	Notes
Storage Temperature	ºC	-45		80	
Operating Relative Humidity	%			85	
Power Supply not Damaged Voltage	V	-0.5		3.6	

Recommended Operating Conditions					
Parameter	Unit	Min.	Typical	Max.	Notes
Operating Case Temperature	ºC	0		70	
Power Supply Working Voltage	V	3.135	3.3	3.465	
Bit Rate	Gbps		400		

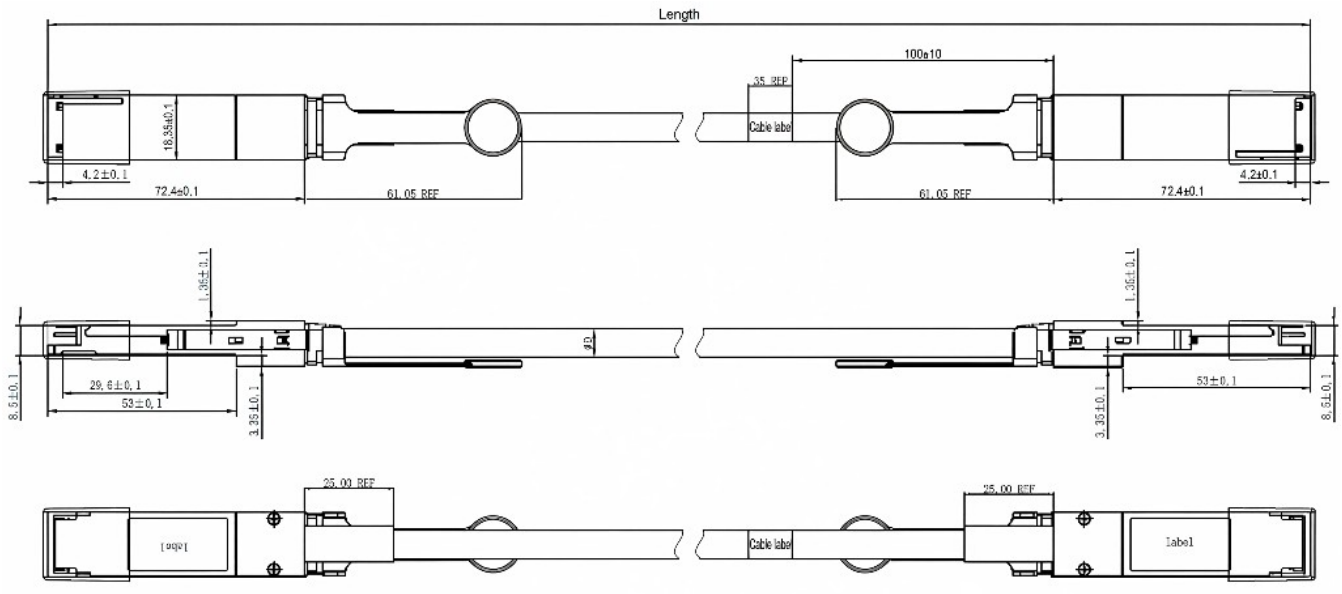
PIN Function Definitions				
Pin #	Symbol	Level/Logic	Description	Notes
1	GND		Ground	
2	TX2n	CML-I	Transmitter Inverted Data Input	
3	TX2p	CML-I	Transmitter Non-Inverted Data Input	
4	GND		Ground	
5	TX4n	CML-I	Transmitter Inverted Data Input	
6	TX4p	CML-I	Transmitter Non-Inverted Data Input	
7	GND		Ground	
8	ModSelL	LVTTL-I	Select	
9	ResetL	LVTTL-I	Reset	
10	Vcc Rx		+3.3 V Power supply receiver	
11	SCL	LVCMOS-I/O	2-wire serial interface clock	
12	SDA	LVCMOS-I/O	2-wire serial interface data	
13	GND		Ground	
14	Rx3p	CML-O	Receiver Non-Inverted Data Output	
15	Rx3n	CML-O	Receiver Inverted Data Output	
16	GND		Ground	
17	Rx1p	CML-O	Receiver Non-Inverted Data Output	
18	Rx1n	CML-O	Receiver Inverted Data Output	
19	GND		Ground	
20	GND		Ground	
21	Rx2n	CML-O	Receiver Inverted Data Output	
22	Rx2p	CML-O	Receiver Non-Inverted Data Output	
23	GND		Ground	
24	Rx4n	CML-O	Receiver Inverted Data Output	
25	Rx4p	CML-O	Receiver Non-Inverted Data Output	
26	GND		Ground	
27	ModPrsL	LVTTL-O	Present	
28	IntL/RxLOS	LVTTL-O	Interrupt/optional RxLOS	
29	Vcc Tx		+3.3 V Power supply transmitter	
30	Vcc1		+3.3 V Power Supply	
31	LPMode/TxD is	LVTTL-I	Low Power Mode/optional TX Disable	
32	GND		Ground	
33	Tx3p	CML-I	Transmitter Non-Inverted Data Input	
34	Tx3n	CML-I	Transmitter Inverted Data Input	
35	GND		Ground	
36	Tx1p	CML-I	Transmitter Non-Inverted Data Input	
37	Tx1n	CML-I	Transmitter Inverted Data Input	
38	GND		Ground	

Transceiver Electrical Pad Layout

For detail mechanical information, please refer to the related document of QSFP112 MSA



Mechanical Specifications



EEPROM Information

The digital diagnostic memory map specific data field defined as following. For detail EEPROM information, please refer to the related document of CMIS5.2.

