800G OSFP to 2x400G OSFP-RHS AEC
Active Electrical Cable

Overview

The Wave2Wave 800G OSFP to 2×400G OSFP-RHS Active Electrical Cable (AEC) is engineered to support the accelerating bandwidth demands of next-generation data center architectures. Designed for seamless interoperability across OSFP platforms, this high-performance breakout solution enables low-latency, power-efficient 800G to dual-400G connectivity in short-reach environments.



Fully compliant with OSFP MSA and CMIS 5.2, the cable ensures consistent signal integrity, robust thermal performance, and reliable integration across switches, servers, and high-density compute systems. With flexible cable gauges, extended link options, and optimized power consumption, it provides a scalable pathway for modern cloud, AI/ML, and hyperscale deployments.

Features & Benefits

- Standards-compliant 800G to 2×400G OSFP-RHS breakout with OSFP MSA and CMIS 5.2
- High-quality signal performance with post-FEC BER $<1\times10^{-15}$
- Low-power architecture: <12W (800G side) and <6.5W (400G side)
- Cable gauge options (26/28/30/32 AWG) with lengths up to 7m
- Single +3.3V power design for streamlined integration
- Reliable 0°C–70°C operation for data center environments
- Broad interoperability with OSFP-based platforms
- RoHS-compliant for sustainable deployments

Applications

- Hyperscale and cloud data centers
- AI/ML compute clusters and high-density fabrics
- Switch-to-switch and switch-to-server aggregation links
- Storage, routing, and high-performance computing environments

Absolute Maximum Ratings

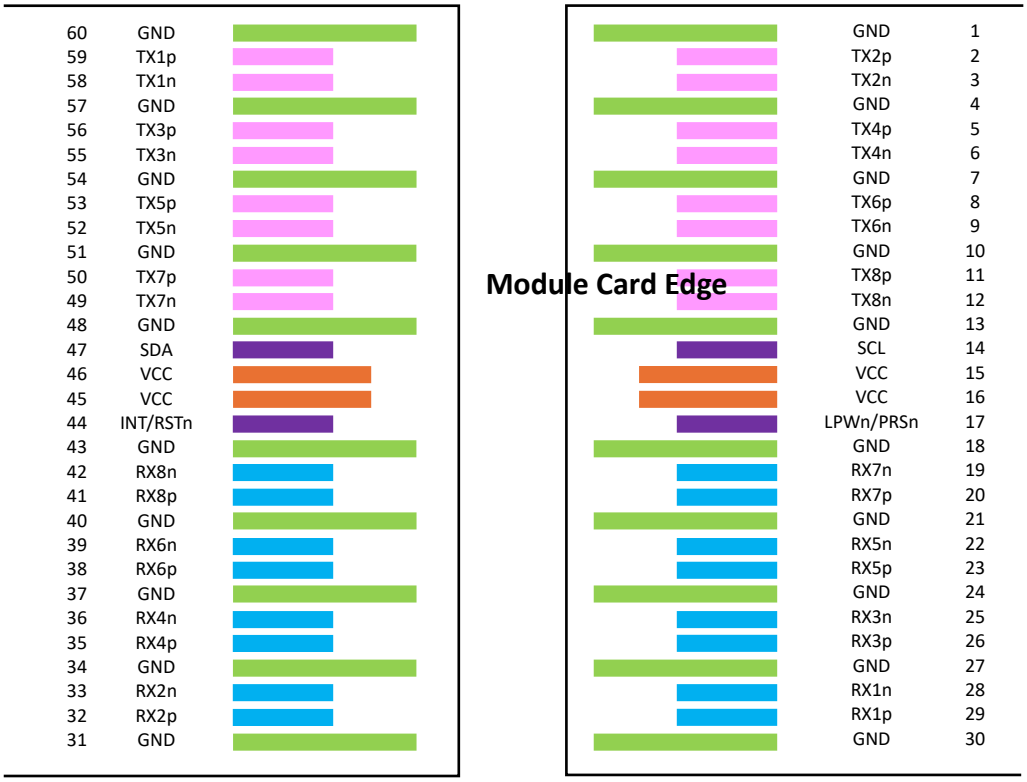
Parameter	Unit	Min.	Typical	Max.	Notes
Storage Temperature	ºC	-45		80	
Operating Relative Humidity	%			85	
Power Supply not Damaged Voltage	V	-0.5		3.6	

Recommended Operating Conditions					
Parameter	Unit	Min.	Typical	Max.	Notes
Operating Case Temperature	ºC	0		70	
Power Supply Working Voltage	V	3.135	3.3	3.465	
Bit Rate	Gbps		800		

PIN Function Definitions						
Pin #	Symbol	Description	Logic	Direction	Plug Sequence	Notes
1	GND	Ground			1	
2	TX2p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
3	TX2n	Transmitter Data Inverted	CML-I	Input from Host	3	
4	GND	Ground			1	
5	TX4p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
6	TX4n	Transmitter Data Inverted	CML-I	Input from Host	3	
7	GND	Ground			1	
8	TX6p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
9	TX6n	Transmitter Data Inverted	CML-I	Input from Host	3	
10	GND	Ground			1	
11	TX8p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
12	TX8n	Transmitter Data Inverted	CML-I	Input from Host	3	
13	GND	Ground			1	
14	SCL	2-wire Serial interface clock	LVCMOS-I/O	Bi-directional	3	Open-Drain with pull-up resistor on Host
15	VCC	+3.3V Power		Power from Host	2	
16	VCC	+3.3V Power		Power from Host	2	
17	LPWn/ PRSn	Low-Power Mode / Module Present	Multi-Level	Bi-directional	3	See pin description for required circuit
18	GND	Ground			1	
19	RX7n	Receiver Data Inverted	CML-O	Output to Host	3	
20	RX7p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
21	GND	Ground			1	
22	RX5n	Receiver Data Inverted	CML-O	Output to Host	3	
23	RX5p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
24	GND	Ground			1	
25	RX3n	Receiver Data Inverted	CML-O	Output to Host	3	
26	RX3p	Receiver Data Non-Inverted	CML-O	Output to Host	3	

PIN Function Definitions (Continued)						
Pin #	Symbol	Description	Logic	Direction	Plug Sequence	Notes
27	GND	Ground			1	
28	RX1n	Receiver Data Inverted	CML-O	Output to Host	3	
29	RX1p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
30	GND	Ground			1	
31	GND	Ground			1	
32	RX2p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
33	RX2n	Receiver Data Inverted	CML-O	Output to Host	3	
34	GND	Ground			1	
35	RX4p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
36	RX4n	Receiver Data Inverted	CML-O	Output to Host	3	
37	GND	Ground			1	
38	RX6p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
39	RX6n	Receiver Data Inverted	CML-O	Output to Host	3	
40	GND	Ground			1	
41	RX8p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
42	RX8n	Receiver Data Inverted	CML-O	Output to Host	3	
43	GND	Ground			1	
44	INT/RSTn	Module Interrupt / Module Reset	Multi-Level	Bi-directional	3	See pin description for required circuit
45	VCC	+3.3V Power		Power from Host	2	
46	VCC	+3.3V Power		Power from Host	2	
47	SDA	2-wire Serial interface data	LVCMOS-I/O	Bi-directional	3	Open-Drain with pull-up resistor on Host
48	GND	Ground			1	
49	TX7n	Transmitter Data Inverted	CML-I	Input from Host	3	
50	TX7p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
51	GND	Ground			1	
52	TX5n	Transmitter Data Inverted	CML-I	Input from Host	3	
53	TX5p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
54	GND	Ground			1	
55	TX3n	Transmitter Data Inverted	CML-I	Input from Host	3	
56	TX3p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
57	GND	Ground			1	
58	TX1n	Transmitter Data Inverted	CML-I	Input from Host	3	
59	TX1p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
60	GND	Ground			1	

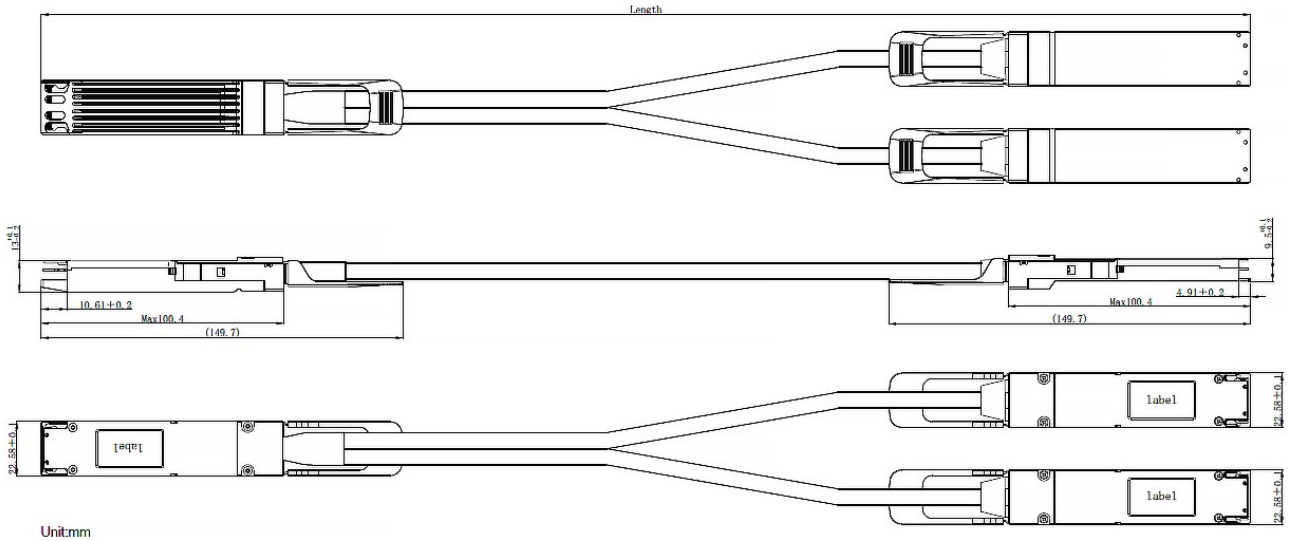
Electrical Pad Layout



Top Side (viewed from top) **Bottom Side (viewed from bottom)**

Mechanical Outlines

For detail mechanical information, please refer to the related document of OSFP MSA.



EEPROM Information

The digital diagnostic memory map specific data field defined as following. For detail EEPROM information, please refer to the related document of CMIS5.2.

