800G OSFP to 4x200G QSFP112 AEC
Active Electrical Cable

Overview

The Wave2Wave 800G OSFP-to-4×200G QSFP112 AEC delivers high-density breakout connectivity for next-generation switching and compute systems. Using 8×112G PAM4 lanes, it provides a full 800Gb/s electrical link on the OSFP side, breaking out to 4×200G QSFP112 interfaces for efficient fan-out in AI/ML clusters and spine–leaf architectures.

Active equalization ensures robust signal integrity across multiple AWG options with lengths up to 7 meters. Fully compliant with OSFP MSA, QSFP112 MSA, and CMIS 5.2, the cable supports predictable link training and stable management operation. Powered from a single 3.3V supply, it operates reliably from 0°C to 70°C in dense thermal environments.

Features & Benefits

- Compliant with OSFP MSA, QSFP112 MSA, and CMIS 5.2 for reliable interoperability
- Supports 800G to 4×200G breakout using 8×112G PAM4 electrical lanes
- Multiple AWG options (26–32AWG) optimized for insertion loss and flexibility
- Lengths up to 7m, depending on AWG and host channel budget
- Power consumption: <12W OSFP side and <3.5W per QSFP112
- Single 3.3V operation for simplified system integration
- Post-FEC BER < 1×10^{-15} for stable PAM4 performance
- Operating case temperature: 0°C to 70°C, suitable for dense thermal environments
- Fully RoHS compliant

Applications

- High-density data-center fabrics
- 800G to 4×200G TOR and leaf/spine breakout
- AI/ML cluster interconnects
- Switch-to-switch and switch-to-server fan-out links
- Short-reach electrical aggregation architectures

Absolute Maximum Ratings

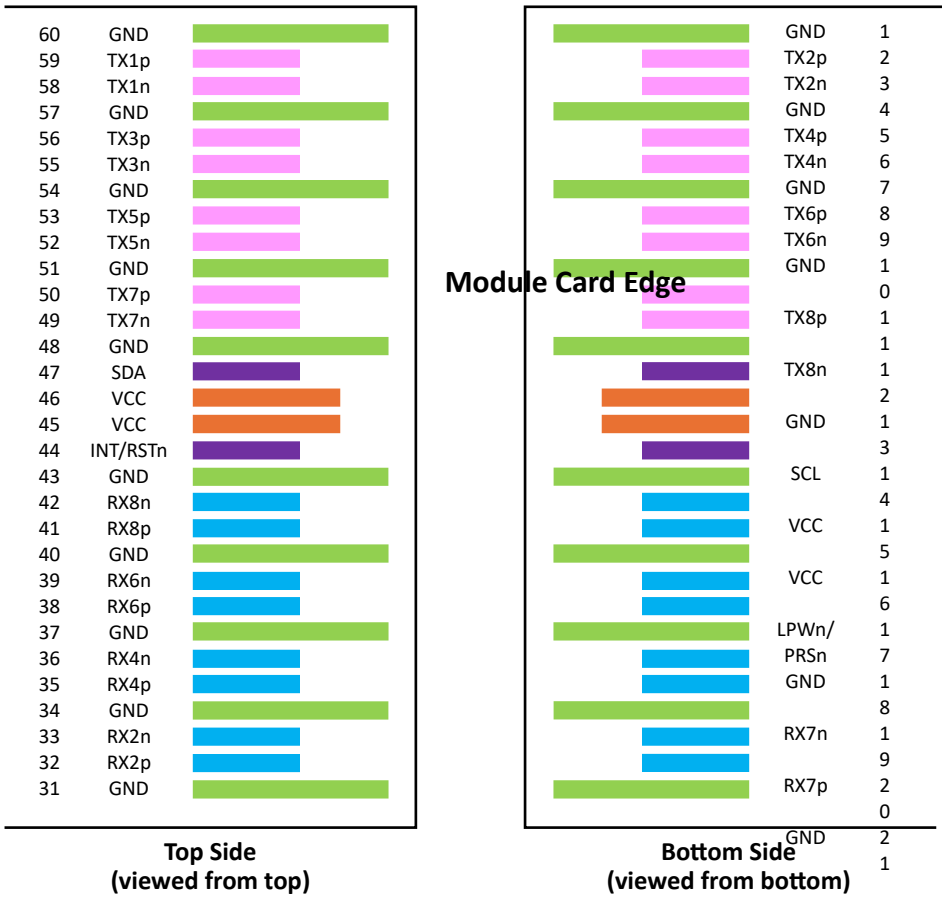
Parameter	Unit	Min.	Typical	Max.	Notes
Storage Temperature	ºC	-45		80	
Operating Relative Humidity	%			85	
Power Supply not Damaged Voltage	V	-0.5		3.6	

Recommended Operating Conditions					
Parameter	Unit	Min.	Typical	Max.	Notes
Operating Case Temperature	ºC	0		70	
Power Supply Working Voltage	V	3.135	3.3	3.465	
Bit Rate	Gbps		800		

OSFP Pin Function Definitions						
Pin #	Symbol	Description	Logic	Direction	Plug Sequence	Notes
1	GND	Ground			1	
2	TX2p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
3	TX2n	Transmitter Data Inverted	CML-I	Input from Host	3	
4	GND	Ground			1	
5	TX4p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
6	TX4n	Transmitter Data Inverted	CML-I	Input from Host	3	
7	GND	Ground			1	
8	TX6p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
9	TX6n	Transmitter Data Inverted	CML-I	Input from Host	3	
10	GND	Ground			1	
11	TX8p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
12	TX8n	Transmitter Data Inverted	CML-I	Input from Host	3	
13	GND	Ground			1	
14	SCL	2-wire Serial interface clock	LVCMOS-I/O	Bi-directional	3	Open-Drain with pull-up resistor on Host
15	VCC	+3.3V Power		Power from Host	2	
16	VCC	+3.3V Power		Power from Host	2	
17	LPWn/ PRSn	Low-Power Mode / Module Present	Multi-Level	Bi-directional	3	See pin description for required circuit
18	GND	Ground			1	
19	RX7n	Receiver Data Inverted	CML-O	Output to Host	3	
20	RX7p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
21	GND	Ground			1	
22	RX5n	Receiver Data Inverted	CML-O	Output to Host	3	
23	RX5p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
24	GND	Ground			1	
25	RX3n	Receiver Data Inverted	CML-O	Output to Host	3	
26	RX3p	Receiver Data Non-Inverted	CML-O	Output to Host	3	

OSFP PIN Function Definitions (Continued)						
Pin #	Symbol	Description	Logic	Direction	Plug Sequence	Notes
27	GND	Ground			1	
28	RX1n	Receiver Data Inverted	CML-O	Output to Host	3	
29	RX1p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
30	GND	Ground			1	
31	GND	Ground			1	
32	RX2p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
33	RX2n	Receiver Data Inverted	CML-O	Output to Host	3	
34	GND	Ground			1	
35	RX4p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
36	RX4n	Receiver Data Inverted	CML-O	Output to Host	3	
37	GND	Ground			1	
38	RX6p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
39	RX6n	Receiver Data Inverted	CML-O	Output to Host	3	
40	GND	Ground			1	
41	RX8p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
42	RX8n	Receiver Data Inverted	CML-O	Output to Host	3	
43	GND	Ground			1	
44	INT/RSTn	Module Interrupt / Module Reset	Multi-Level	Bi-directional	3	See pin description for required circuit
45	VCC	+3.3V Power		Power from Host	2	
46	VCC	+3.3V Power		Power from Host	2	
47	SDA	2-wire Serial interface data	LVCMOS-I/O	Bi-directional	3	Open-Drain with pull-up resistor on Host
48	GND	Ground			1	
49	TX7n	Transmitter Data Inverted	CML-I	Input from Host	3	
50	TX7p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
51	GND	Ground			1	
52	TX5n	Transmitter Data Inverted	CML-I	Input from Host	3	
53	TX5p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
54	GND	Ground			1	
55	TX3n	Transmitter Data Inverted	CML-I	Input from Host	3	
56	TX3p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
57	GND	Ground			1	
58	TX1n	Transmitter Data Inverted	CML-I	Input from Host	3	
59	TX1p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
60	GND	Ground			1	

OSFP Electrical Pad Layout

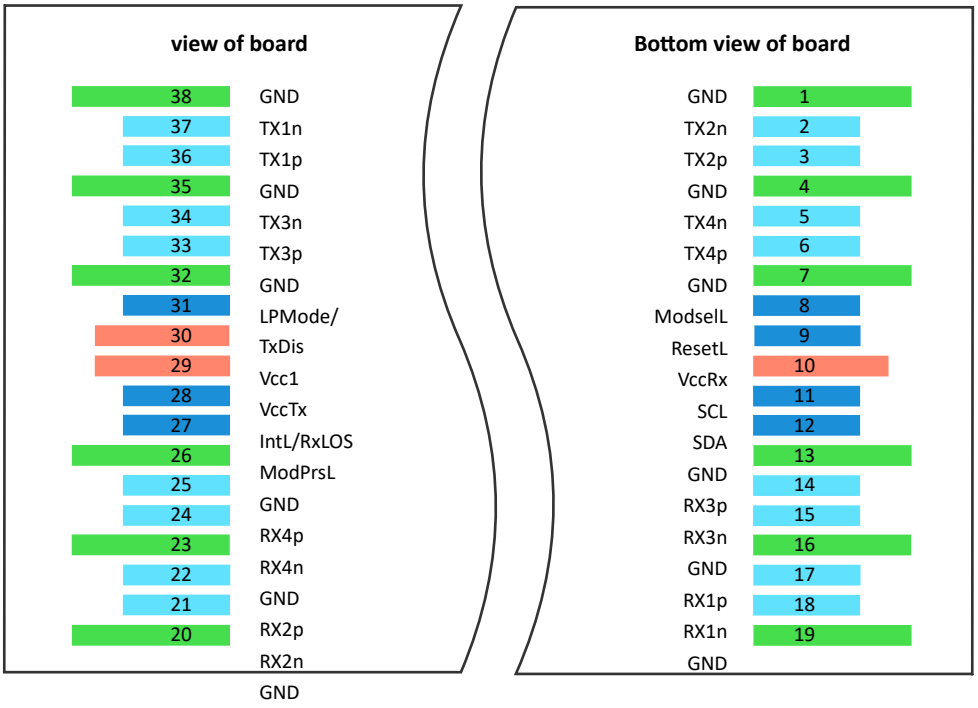


OSFP112 PIN Function Definitions

Pin #	Symbol	Level/Logic	Description	Notes
1	GND		Ground	
2	TX2n	CML-I	Transmitter Inverted Data Input	
3	TX2p	CML-I	Transmitter Non-Inverted Data Input	
4	GND		Ground	
5	TX4n	CML-I	Transmitter Inverted Data Input	
6	TX4p	CML-I	Transmitter Non-Inverted Data Input	
7	GND		Ground	
8	ModSelL	LVTTL-I	Select	
9	ResetL	LVTTL-I	Reset	
10	Vcc Rx		+3.3 V Power supply receiver	
11	SCL	LVCMOS-I/O	2-wire serial interface clock	
12	SDA	LVCMOS-I/O	2-wire serial interface data	
13	GND		Ground	
14	Rx3p	CML-O	Receiver Non-Inverted Data Output	
15	Rx3n	CML-O	Receiver Inverted Data Output	

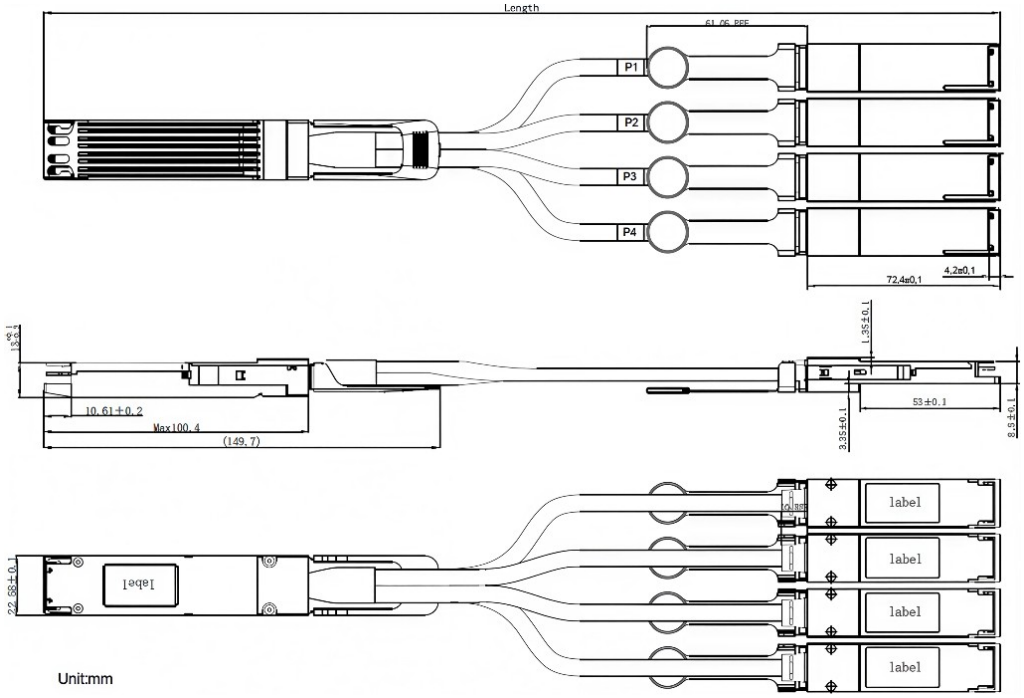
OSFP112 PIN Function Definitions (Continued)				
Pin #	Symbol	Level/Logic	Description	Notes
16	GND		Ground	
17	Rx1p	CML-O	Receiver Non-Inverted Data Output	
18	Rx1n	CML-O	Receiver Inverted Data Output	
19	GND		Ground	
20	GND		Ground	
21	Rx2n	CML-O	Receiver Inverted Data Output	
22	Rx2p	CML-O	Receiver Non-Inverted Data Output	
23	GND		Ground	
24	Rx4n	CML-O	Receiver Inverted Data Output	
25	Rx4p	CML-O	Receiver Non-Inverted Data Output	
26	GND		Ground	
27	ModPrsL	LVTTL-O	Present	
28	IntL/RxLOS	LVTTL-O	Interrupt/optional RxLOS	
29	Vcc Tx		+3.3 V Power supply transmitter	
30	Vcc1		+3.3 V Power Supply	
31	LPMode/TxD is	LVTTL-I	Low Power Mode/optional TX Disable	
32	GND		Ground	
33	Tx3p	CML-I	Transmitter Non-Inverted Data Input	
34	Tx3n	CML-I	Transmitter Inverted Data Input	
35	GND		Ground	
36	Tx1p	CML-I	Transmitter Non-Inverted Data Input	
37	Tx1n	CML-I	Transmitter Inverted Data Input	
38	GND		Ground	

QSFP112 Transceiver Electrical Pad Layout



Mechanical Outlines

For detail mechanical information, please refer to the related document of OSFP MSA and QSFP112 MSA



EEPROM Information

The digital diagnostic memory map specific data field defined as following. For detail EEPROM information, please refer to the related document of CMIS5.2.

