800G QSFP-DD to 800G QSFP-DD AEC
Active Electrical Cable

Overview

The Wave2Wave 800G QSFP-DD to QSFP-DD Active Electrical Cable (AEC) provides high-bandwidth, short-reach electrical connectivity for next-generation switching, routing, and compute platforms. Built on 8×112G PAM4 lanes, the assembly delivers a full 800Gb/s link with active equalization to maintain signal integrity across challenging electrical channels.

Fully compliant with IEEE 802.3ck, QSFP-DD MSA, and CMIS 5.2, the cable ensures predictable host interoperability, accurate management interface behavior, and robust PAM4 performance. Supporting lengths up to 6 meters, the AEC operates from a single 3.3V rail, features power consumption below 12W per end, and maintains post-FEC BER < 1×10^{-15} across the full 0°C to 70°C operating range.

Features & Benefits

- Compliant with IEEE 802.3ck, QSFP-DD MSA, and CMIS 5.2 for consistent interoperability
- Supports 8×112G PAM4 lanes delivering full 800Gb/s performance
- Multiple AWG options (28/30/32AWG) optimized for reach, loss, and bend flexibility
- Link lengths up to 6m, depending on gauge and host channel budget
- Low power usage under 12W per end on a 3.3V supply
- Post-FEC BER < 1×10^{-15} ensuring stable PAM4 signal integrity
- Operating case temperature 0°C to 70°C for dense front-panel environments
- Fully RoHS compliant

Applications

- High-density data-center fabrics
- HPC, AI/ML compute clusters
- Switch-to-switch and switch-to-server interconnects
- Router, server, and storage platforms requiring 800G electrical links

Absolute Maximum Ratings

Parameter	Unit	Min.	Typical	Max.	Notes
Storage Temperature	ºC	-45		80	
Operating Relative Humidity	%			85	
Power Supply not Damaged Voltage	V	-0.5		3.6	

Recommended Operating Conditions					
Parameter	Unit	Min.	Typical	Max.	Notes
Operating Case Temperature	ºC	0		70	
Power Supply Working Voltage	V	3.135	3.3	3.465	
Power consumption per end	W			12	
Bit Rate	Gbps		800		

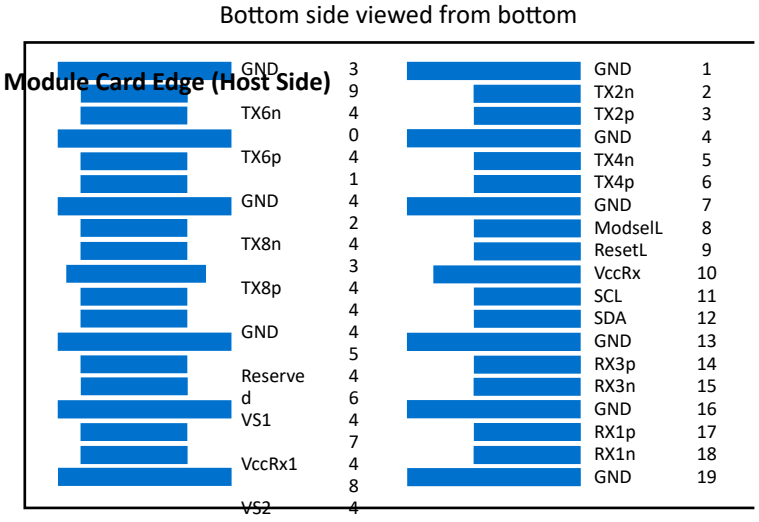
PIN Function Definitions				
Pin #	Symbol	Level/Logic	Description	Notes
1	GND		Module Ground	
2	Tx2n	CML-I	Transmitter Inverted Data Input	
3	Tx2p	CML-I	Transmitter Non-Inverted Data Input	
4	GND		Module Ground	
5	Tx4n	CML-I	Transmitter Inverted Data Input	
6	Tx4p	CML-I	Transmitter Non-Inverted Data Input	
7	GND		Module Ground	
8	ModSelL	LVTTL-I	Module Select	
9	ResetL	LVTTL-I	Module Reset	
10	VccRx		+3.3V Power Supply for Receiver	
11	SCL	LVTTL-I	2-Wire Serial Interface Clock	
12	SDA	LVTTL-I/O	2-Wire Serial Interface Data Line	
13	GND		Module Ground	
14	Rx3p	CML-O	Receiver Non-Inverted Data Output	
15	Rx3n	CML-O	Receiver Inverted Data Output	
16	GND		Module Ground	
17	Rx1p	CML-O	Receiver Non-Inverted Data Output	
18	Rx1n	CML-O	Receiver Inverted Data Output	
19	GND		Module Ground	
20	GND		Module Ground	
21	Rx2n	CML-O	Receiver Inverted Data Output	
22	Rx2p	CML-O	Receiver Non-Inverted Data Output	
23	GND		Module Ground	
24	Rx4n	CML-O	Receiver Inverted Data Output	
25	Rx4p	CML-O	Receiver Non-Inverted Data Output	
26	GND		Module Ground	
27	ModPrsL	LVTTL-O	Module Present	
28	IntL/RxLOSL	LVTTL-O	Interrupt. Optionally configurable as RxLOSL via the management interface	
29	VccTx		+3.3V Power Supply for Transmitter	
30	Vcc1		+3.3V Power Supply	

PIN Function Definitions (continued)				
Pin #	Symbol	Level/Logic	Description	Notes
31	LPMode/TxDis	LVTTL-I	Low Power Mode. Optionally configurable as TxDis via the management interface	
32	GND		Module Ground	
33	Tx3p	CML-I	Transmitter Non-Inverted Data Input	
34	Tx3n	CML-I	Transmitter Inverted Data Input	
35	GND		Module Ground	
36	Tx1p	CML-I	Transmitter Non-Inverted Data Input	
37	Tx1n	CML-I	Transmitter Inverted Data Input	
38	GND		Module Ground	
39	GND		Module Ground	
40	Tx6n	CML-I	Transmitter Inverted Data Input	
41	Tx6p	CML-I	Transmitter Non-Inverted Data Input	
42	GND		Module Ground	
43	Tx8n	CML-I	Transmitter Inverted Data Input	
44	Tx8p	CML-I	Transmitter Non-Inverted Data Input	
45	GND		Module Ground	
46	Reserved		For future use	
47	VSI		Module Vendor Specific 1	
48	VccRx1		3.3V Power Supply	
49	VS2		Module Vendor Specific 2	
50	VS3		Module Vendor Specific 3	
51	GND		Module Ground	
52	Rx7p	CML-O	Receiver Non-Inverted Data Output	
53	Rx7n	CML-O	Receiver Inverted Data Output	
54	GND		Module Ground	
55	Rx5p	CML-O	Receiver Non-Inverted Data Output	
56	Rx5n	CML-O	Receiver Inverted Data Output	
57	GND		Module Ground	
58	GND		Module Ground	
59	Rx6n	CML-O	Receiver Inverted Data Output	
60	Rx6p	CML-O	Receiver Non-Inverted Data Output	
61	GND		Module Ground	
62	Rx8n	CML-O	Receiver Inverted Data Output	
63	Rx8p	CML-O	Receiver Non-Inverted Data Output	
64	GND		Module Ground	
65	NC		No Connect	
66	Reserved		For future use	
67	VccTx1		3.3V Power Supply	
68	Vcc2		3.3V Power Supply	
69	Reserved		For future use	

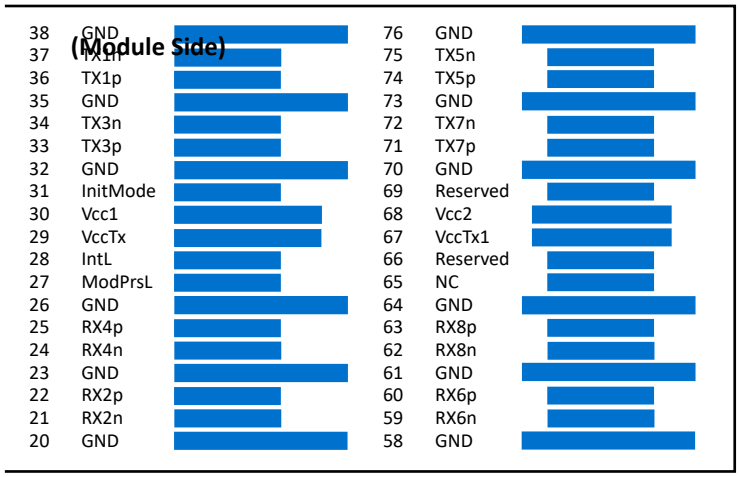
PIN Function Definitions (continued)				
Pin #	Symbol	Level/Logic	Description	Notes
70	GND		Module Ground	
71	Tx7p	CML-I	Transmitter Non-Inverted Data Input	
72	Tx7n	CML-I	Transmitter Inverted Data Input	
73	GND		Module Ground	
74	Tx5p	CML-I	Transmitter Non-Inverted Data Input	
75	Tx5n	CML-I	Transmitter Inverted Data Input	
76	GND		Module Ground	

Electrical Pad Layout

Bottom side viewed from bottom

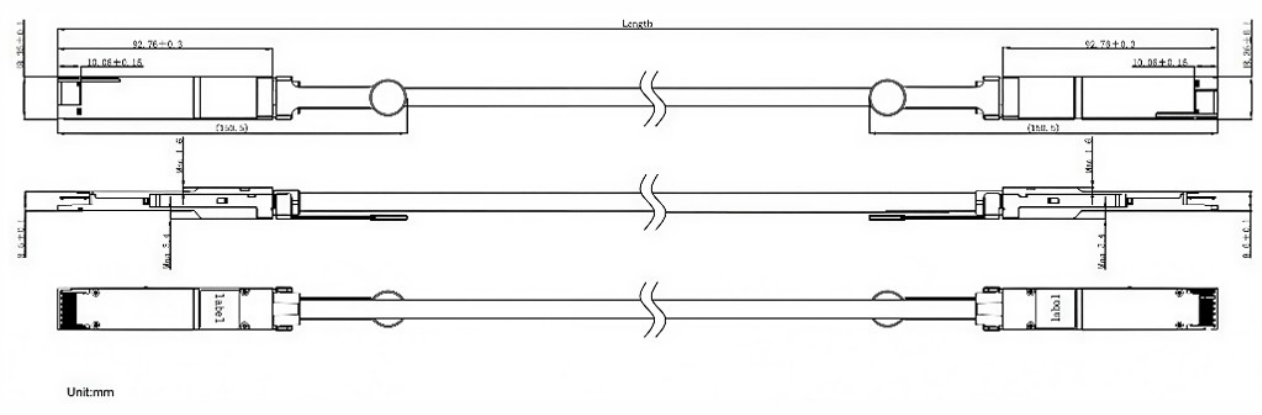


Top side viewed from top



Mechanical Outlines

For detail mechanical information, please refer to the related document of QSFP-DD MSA.



EEPROM Information

The digital diagnostic memory map specific data field defined as following. For detail EEPROM information, please refer to the related document of CMIS5.2.

